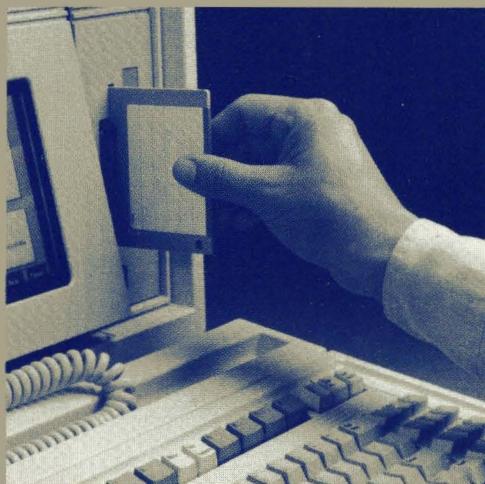


HEWLETT-PACKARD



**HP 82919A Serial Interface
Owner's Manual**

HP 82919A Serial Interface Owner's Manual



Edition 1 August 1984

Reorder Number

82919-90001

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Specifications

Transmission Mode	Serial, asynchronous—simplex, half duplex, or full duplex.
Baud Rate	Up to 19,200.*
Back-Panel Connector	Male 25-pin D-subminiature, configured as DTE.
Drivers and Receivers	In accord with EIA standard RS-232-C.†
Dimensions	Approximately 19.1 by 13.5 by 2.7 cm (7.5 by 5.3 by 1.1 in.).
Weight	218 g (7.7 oz).
Operating Temperature	0° to 40°C (32° to 104°F).
Storage Temperature	–40° to 75°C (–40° to 167°F).
Operating Humidity	5% to 95% relative humidity at 40°C.

* Your computer's operating system may limit the baud rate to 9,600.

† Refer to EIA standard RS-232-C, "Interface Between Data Terminal Equipment and Data Communication Equipment Employing Serial Binary Data Interchange," adopted October 1969 and reaffirmed June 1981, Electronic Industries Association, Washington, D.C.

Potential for Radio/ Television Interference (for U.S.A. Only)

The HP 82919A Serial Interface generates and uses radio frequency energy and, if not installed and used properly—that is, in strict accordance with the instructions in this manual—may cause interference to radio and television reception. It has been tested and found to comply with the limits for a Class B computing device in accordance with the specifications in Subpart J of Part 15 of FCC rules, which are designed to provide reasonable protection against such interference in a residential installation. However, there is no guarantee that interference will not occur in a particular installation. In the unlikely event that your product does cause interference to radio or television reception (which can be determined by turning off the computer, removing the interface, then turning the computer back on) you are encouraged to try to correct the interference by one or more of the following measures:

- Reorient the receiving antenna.
- Relocate the interface cable with respect to the receiver.
- Move the computer and interface away from the receiver.
- Plug the computer into a different ac outlet so that the computer and the receiver are on different branch circuits.

If necessary, you should consult your dealer or an experienced radio/television technician for additional suggestions. You may find the following booklet, prepared by the Federal Communications Commission, helpful: *How to Identify and Resolve Radio-TV Interference Problems*. This booklet is available from the U.S. Government Printing Office, Washington, D.C. 20402, Stock Number 004-000-00345-4.

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1

Setting Up the Interface

This chapter shows how to install the HP 82919A Serial Interface and connect a serial peripheral device. *Once you have connected a peripheral, read "Where To Go From Here" at the end of the chapter to determine where to turn for further instructions.*

Unpacking and Inspection

Before you unpack the interface, note that its printed-circuit assembly is exposed. The interface is shipped enclosed in an antistatic bag to protect it against electrostatic discharge (ESD) damage.



Observe the following precautions whenever handling, installing, or removing the interface:

- Whenever you remove your interface from the computer, store it in the original antistatic bag and shipping container.
- Always handle the interface by its metal back panel, not by the exposed circuit board.

Failure to observe these precautions may result in mechanical damage and/or electrostatic discharge (ESD) damage to the interface.

The shipping container should include the following items in addition to this manual:

- HP 82919A Serial Interface.
- Support guide.

Inspect the interface carefully for any signs of shipping damage. Notify your dealer immediately and file a claim with the carriers involved if the interface is damaged or if anything is missing.

Besides the HP 82919A Serial Interface and your computer, you need one of the following cables.

- HP 82974A Modem Cable F/M.
- HP 82974B Instrumentation Cable F/F.
- HP 82974C Serial Printer Cable F/F.
- HP 82974D Serial Printer Cable F/M.



The designation "F/M" indicates a female connector at the interface end and a male connector at the peripheral end of the cable. The designation "F/F" indicates a female connector at both ends of the cable.

Installing the Serial Interface

Note the following precautions before you install the interface.



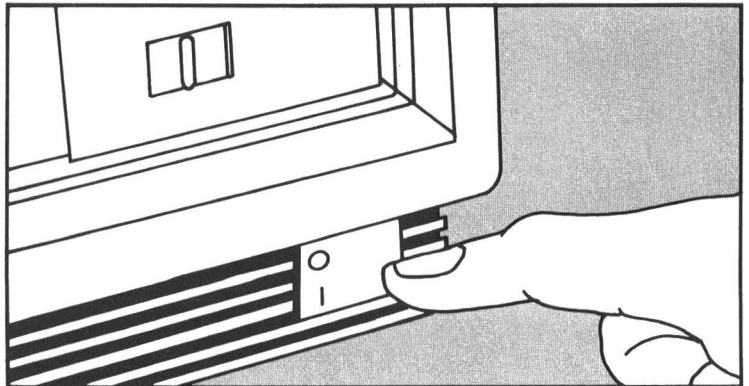
Do not place fingers, tools, or other foreign objects into the plug-in ports of your computer or the connectors of the interface. Such actions may result in minor electrical shock hazard and interference with pacemaker devices worn by some persons. Damage to the connectors and internal circuitry of the computer and/or interface may also result.



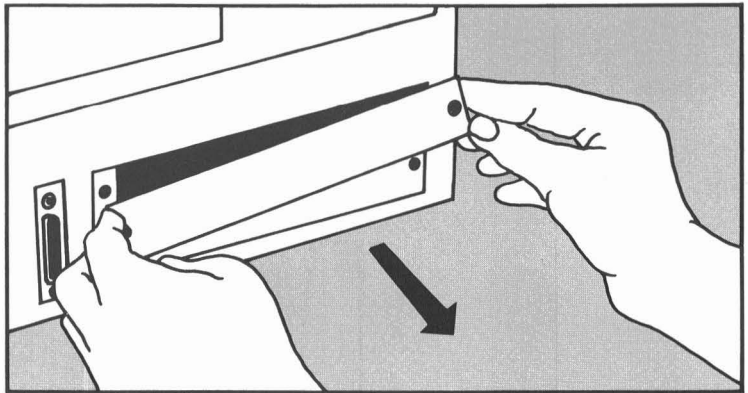
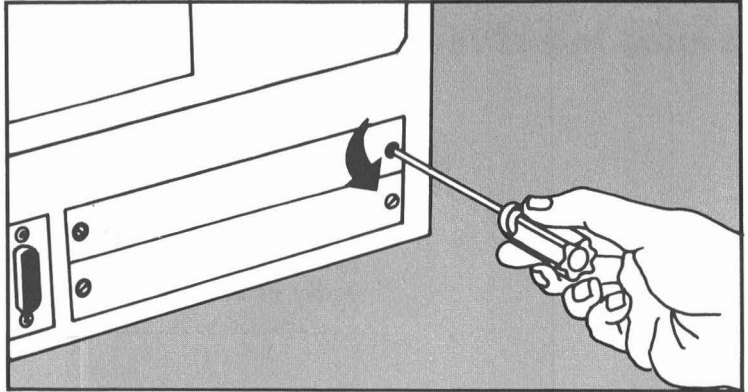
Always turn off the computer and any peripherals connected to it before installing or removing the interface. Failure to observe this procedure may result in damage to the computer, the interface, or both.

To install the interface, follow these steps:

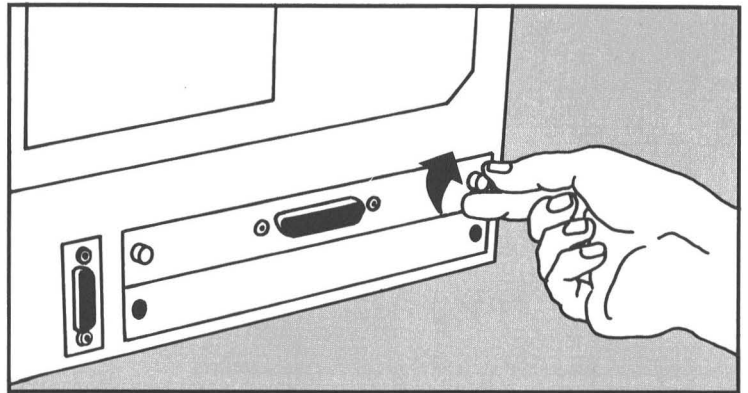
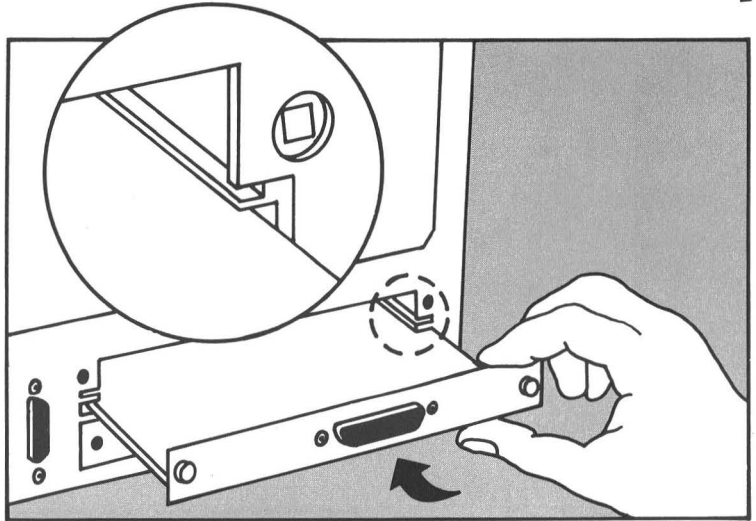
1. Turn off the computer.



2. Uncover an I/O port (on back of computer).

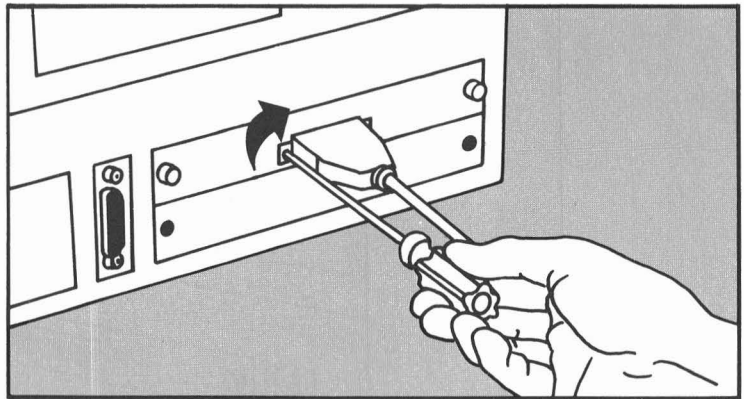
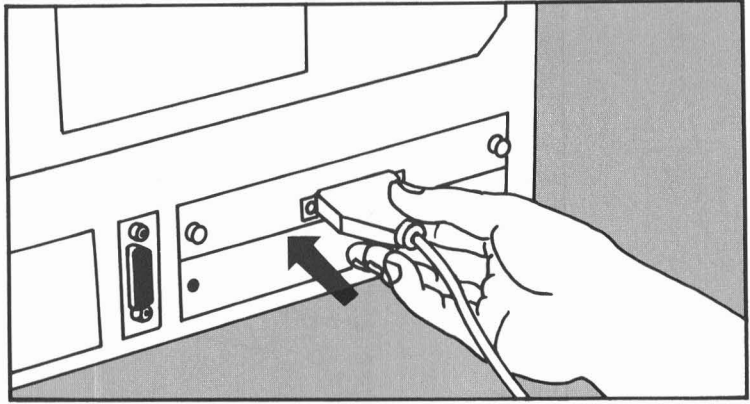


3. Insert the interface.

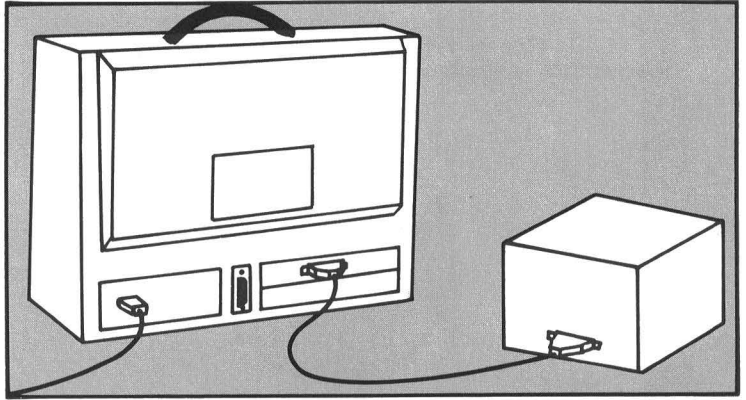


You may install the interface in any unused I/O port. Be sure that the interface is right-side up and that the circuit board is aligned in the guides.

4. Plug in the cable connector.



5. Connect your peripheral.



The cable that you need depends on your peripheral device. Refer to the following section: "Connecting a Peripheral Device."

If you remove the interface for an extended period, replace the cover plate over the I/O port.

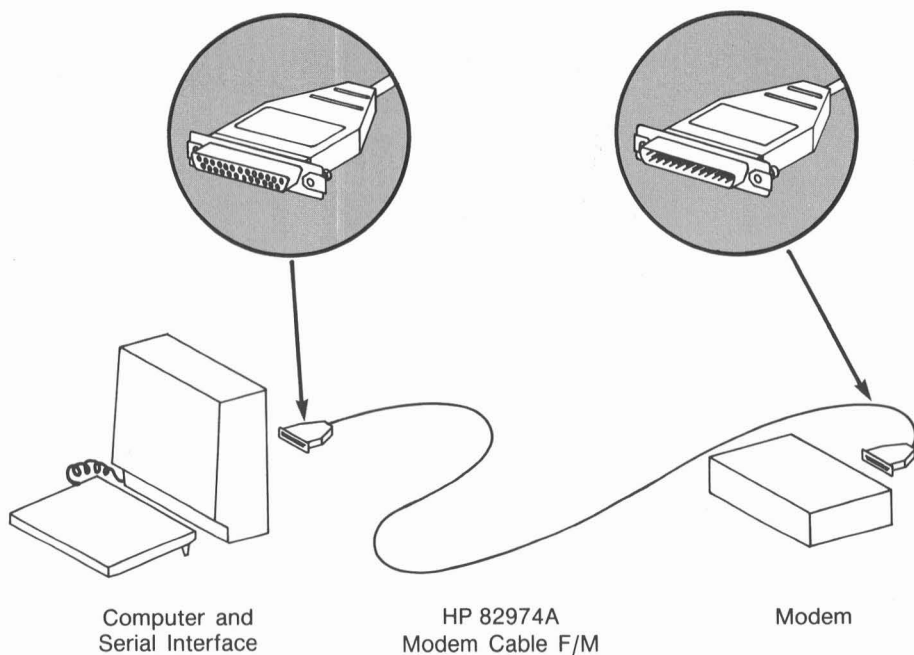
Connecting a Peripheral Device

You can connect most serial peripheral devices to the HP 82919A Serial Interface by using one of the four available cables. The cable that you need depends on your peripheral.

Connecting a Modem

All modems can be connected with the HP 82974A Modem Cable F/M, as shown in figure 1-1:

Figure 1-1.
Connecting a Modem

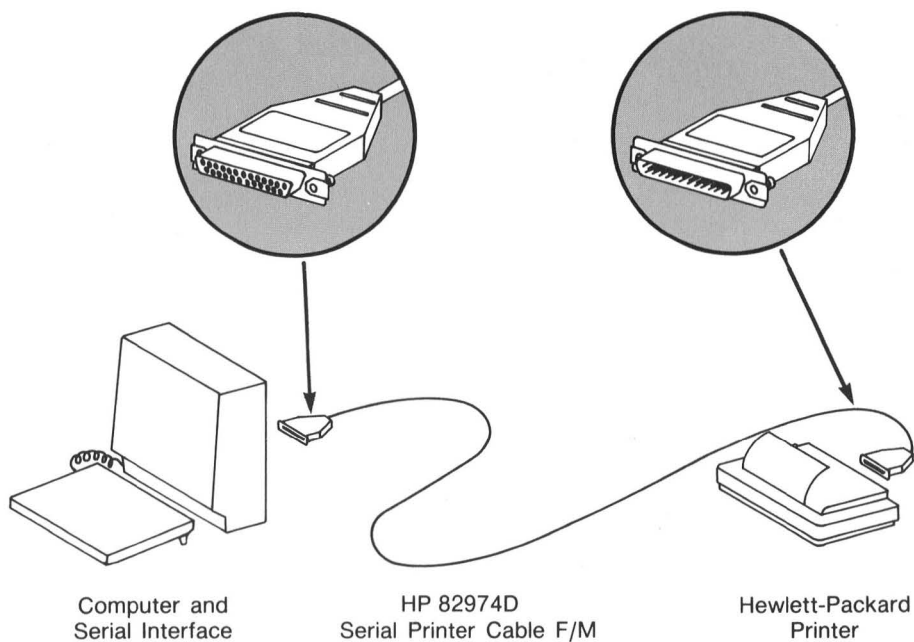


Plug the female connector (shown on the left in the figure) into the serial interface and the male connector (shown on the right) into the modem. Secure each connector with its retainer screws.

Connecting a Hewlett-Packard Printer or Terminal

You can connect a Hewlett-Packard serial printer or terminal with the HP 82974D Serial Printer Cable F/M, as shown in figure 1-2:

Figure 1-2.
Connecting an HP Printer

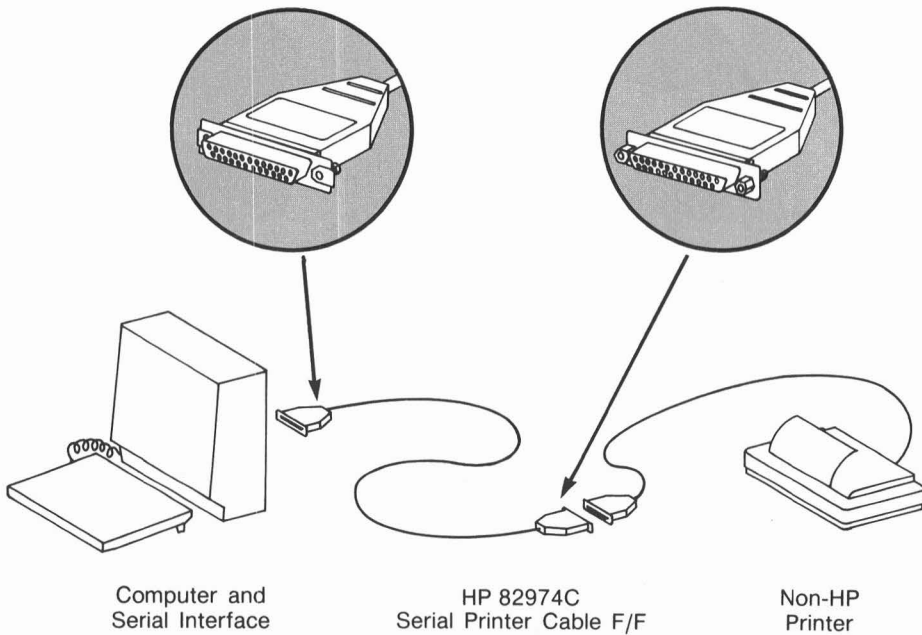


Plug the female connector into the serial interface and the male connector into the printer. Secure each connector with its retainer screws.

Connecting a Non-HP Printer or Terminal

You can use the HP 82974C Serial Printer Cable F/F to connect most serial printers and terminals other than those made by Hewlett-Packard. Figure 1-3 shows a typical configuration:

Figure 1-3.
Connecting a Non-HP Printer



Note that the HP 82974C Serial Printer Cable F/F has female connectors at both ends. The connector at the interface end of the cable has retainer screws (to fasten the connector to the interface's back-panel connector), while the connector at the peripheral end has jack posts (to connect with an in-line male connector). *These connectors are not equivalent.* The pin configuration is different at each end of the cable. You can remove the jack posts from the connector at the peripheral end of the cable if you want to plug it directly into a peripheral device. However, you need to mark the connectors so that you can tell them apart.

Connecting Other Serial Peripherals

If you are connecting a serial peripheral other than a modem, printer, or terminal, you need some technical information about the peripheral in order to select a cable. *To select the proper cable for your application, refer to appendix A.* Appendix A covers the technical details of the four serial interface cables, including the pin configurations.

Where To Go From Here

Once you have installed the serial interface and connected a peripheral, you are ready to use the interface for data communications. However, you need a data communications program to control the input and output of data. The procedure to follow depends upon the program you are using:

- If you are using a Hewlett-Packard data communications program such as "Datacomm," refer to the user's manual supplied with the program.
- If you are writing your own data communications program, refer to your programming language manuals. If you need to access the internal registers of the interface, refer to chapter 2 in this manual.
- If you are writing your own interface driver program, refer to your operating system documentation. Refer to chapter 2 in this manual for a description of the interface hardware, including the internal registers.



Chapter 2 describes the serial interface circuit and hardware registers. It is written for the advanced programmer. You do not need to read chapter 2 unless you want to access the hardware registers directly.

The documentation provided with your computer and its peripherals may also help you.

If you suspect a malfunction, refer to the diagnostic procedures in your computer owner's manual. Refer to the support guide included with the interface for service and warranty information.

2

Hardware Description

This chapter describes the circuitry and internal registers of the HP 82919A Serial Interface. It is intended for the advanced programmer who wants to control the operation of the interface by accessing its internal registers. Read this chapter if you are writing your own serial interface driver program, or if you are writing a data communications program and need to access the internal registers.

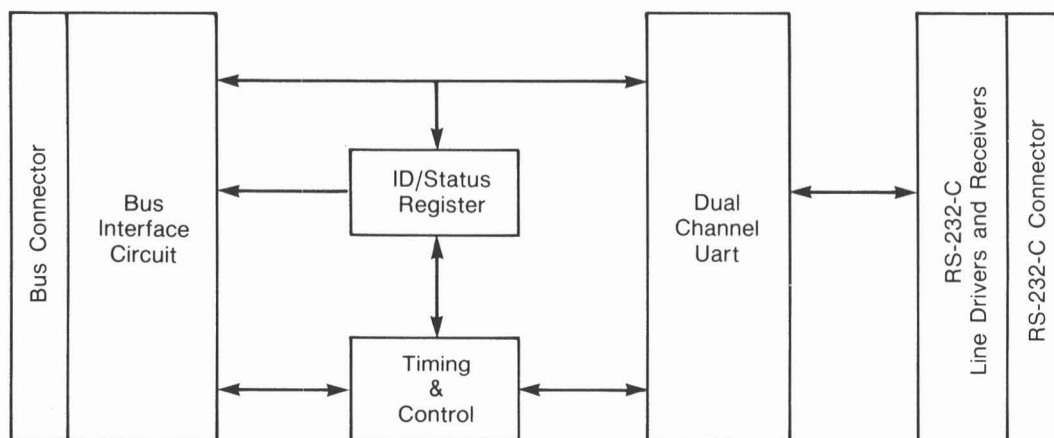
Most users of the serial interface do not need to read this chapter. If you are using a Hewlett-Packard data communications program such as "Datacomm," follow the instructions in the manual provided with the program. If you are programming in HP-UX Technical BASIC, use the registers described in the HP-UX Technical BASIC I/O Programming Guide to control the interface, rather than the registers described here.



Functional Description

Figure 2-1 illustrates the major components of the HP 82919A Serial Interface. The interface uses a dual channel UART (Universal Asynchronous Receiver Transmitter) to convert transmitted data to serial form and to convert incoming serial characters to parallel form.

Figure 2-1.
Interface Block Diagram



Let's look at each component in turn.

Bus Connector and Interface Circuit

The interface bus connector plugs into the I/O backplane connector on your computer. The bus interface circuit decodes addresses, generates and responds to handshaking signals, and provides data buffering.

Identification and Status Register

The Identification and Status register is a read/write register that identifies the serial interface and controls its capability to interrupt the computer. The timing and control circuit controls access to this register. This register is covered in detail in the "Registers" section later in this chapter.

Timing and Control Circuit

The timing and control circuit generates the signals necessary to control the internal components of the HP 82919A Serial Interface (the bus interface circuit, Identification and Status register, and the dual channel UART).

Dual Channel UART

The major component of the HP 82919A Serial Interface is the UART integrated circuit. The UART provides two data channels, general purpose input and output ports, and several registers. You can control the operation of the interface by accessing these registers. Refer to the "Registers" section at the end of this chapter for specific information.

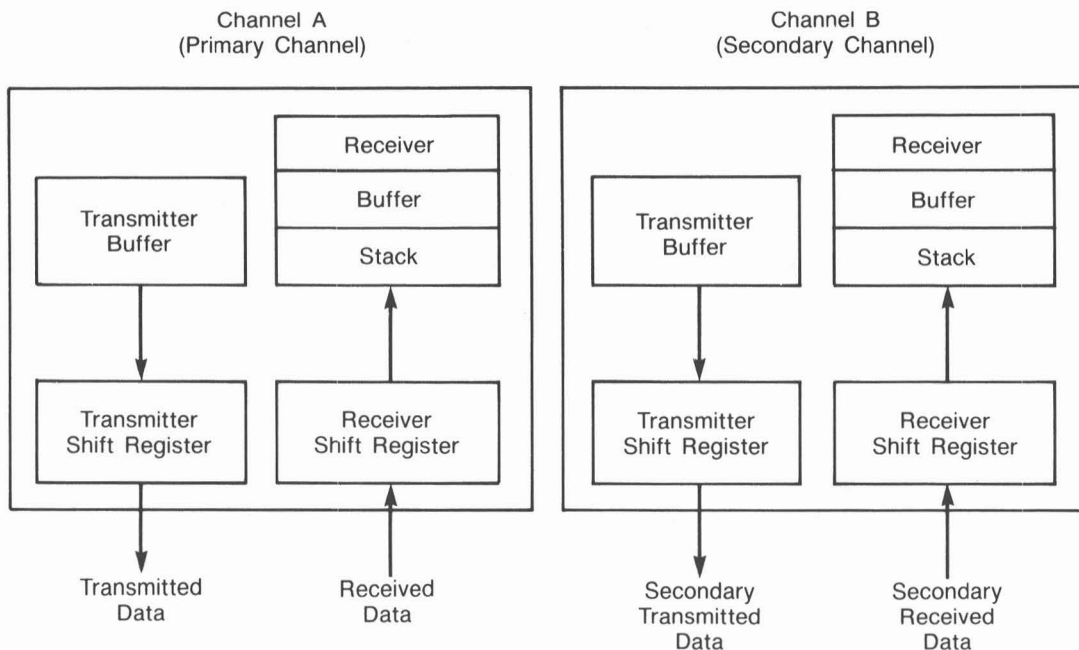
Data Channels. The UART provides two data channels, each with a transmitter and receiver. Channel A (the primary channel) and channel B (the secondary channel) operate independently. You can control the operation of channel A by accessing the channel A mode registers, command register, and status register. You can control channel B by accessing the corresponding registers for that channel. Each channel may operate in a different mode and/or at a different baud rate. The receiver and transmitter within a channel may also operate at different baud rates (in the normal operating mode). You may independently enable the transmitters and receivers of the two channels. If you are using full duplex operation, enable both the transmitter and receiver for the desired channel.



The four available cables do not implement the secondary data channel (channel B). You will need to construct a special cable if you want to use channel B.

Each data channel has a transmitter buffer and shift register, and a receiver buffer and shift register. Figure 2-2 illustrates the operation of the channel A and B transmitters and receivers:

Figure 2-2.
Data Channels



Your program can output data by writing to the transmitter buffer. The data is then transferred to the transmitter shift register, which converts the data to serial form. Incoming serial data is converted to parallel form by the receiver shift register, then transferred to the receiver buffer (a three-character stack). The program can then read the data from the receiver buffer. The following discussion covers transmitter and receiver operation in detail.

Transmitter Operation. Each transmitter, when enabled, indicates that it is ready to accept a character by setting the “transmitter ready” bit in the corresponding status register. You can enable an interrupt for the “transmitter ready” condition. This interrupt is negated when a character is loaded into the transmitter buffer. The character is transferred from the transmitter buffer to the transmitter shift register once the shift register has completed transmission of the previous character. At this point “transmitter ready” is again asserted. Characters cannot be written into the transmitter buffer if the transmitter is disabled.

The transmitter shift register converts the parallel data from the computer to a serial bit stream on the Transmitted Data output. The transmitter automatically sends a start bit, followed by the programmed number of data bits (least-significant bit first), an optional parity bit, and the programmed number of stop bits. Each bit is transmitted as either a *space* (logic 0) or a *mark* (logic 1). If a new character is not available in the transmitter buffer when the stop bits have been sent, the Transmitted Data output remains in the marking (logic 1) state and the “transmitter empty” bit in the status register is set equal to “1”. The “transmitter empty” bit is cleared and transmission resumes when a new character is written into the transmitter buffer by the computer. You can force the transmitter into a continuous spacing (logic 0) condition by issuing a “send break” command.

Receiver Operation. Each receiver, when enabled, searches for a valid start bit. When a start bit is detected, the programmed number of data bits, an optional parity bit, and the programmed number of stop bits are read into the receiver shift register. Each bit is read as either a space (logic 0) or a mark (logic 1). The shift register converts the data into parallel form, the data is transferred to the receiver buffer, and the “receiver ready” bit is set equal to “1” in the status register.

The receiver buffer is a first-in-first-out (FIFO) stack with room for three characters. The first character transferred into the stack by the shift register is the first character read by the computer. Thus, the order of the incoming data is preserved, but buffering for four full characters is provided by the buffer and shift register. The "receiver ready" bit is cleared when the last character in the receiver buffer is read.

If the receiver buffer and receiver shift register are both full and a new character is received, the character in the shift register is overwritten by the new character and the "overrun error" bit is set in the status register. If a parity error, framing error, or received break is detected in the incoming data, the appropriate status bit is set.

Baud Rate Generator and Timer. The UART provides both a baud rate generator and a timer. The baud rate generator provides 18 fixed baud rates. You can also use the timer to provide any desired baud rate in the operating range of the interface (up to 19,200). This baud rate is determined by the divisor contained in Registers 13 and 14. You can independently select baud rates for the transmitters and receivers of the two channels with the channel A and B baud rate select registers (Write Registers 5 and 6). Thus, you may use up to four different baud rates, but only one rate can be provided by the timer.

Input Port. The UART input port provides six general purpose inputs (IP0 through IP5). These inputs are used for control purposes and are connected to the following RS-232-C signal lines in the back-panel connector of the serial interface:

Table 2-1. Input Port Back-Panel Connections

Input Port Pin	RS-232-C Signal Line
IP0	Clear To Send
IP1	Data Set Ready
IP2	Ring Indicator
IP3	Received Line Signal Detector
IP4	Secondary Clear To Send
IP5	Secondary Received Line Signal Detector

The HP 82974A Modem Cable F/M preserves the above configuration except that the two secondary signal lines (IP4 and IP5) are not connected.

The two printer cables reconfigure the input port connections as follows:

Table 2-2. Input Port Printer Cable Connections

Input Port Pin	RS-232-C Signal Line
IP0	Data Terminal Ready
IP1	Data Terminal Ready
IP2	Not Connected
IP3	Request To Send
IP4–IP5	Not Connected

The configuration of the HP 82974B Instrumentation Cable F/F is the same as that of the printer cables except that IP1 is not connected.

Output Port. The UART output port provides eight general purpose outputs (OP0 through OP7). Outputs OP5 through OP7 are not used. Outputs OP0 through OP4 are connected to the following RS-232-C signal lines in the back-panel connector of the serial interface:

Table 2-3. Output Port Back-Panel Connections

Output Port Pin	RS-232-C Signal Line
OP0	Data Terminal Ready
OP1	Request To Send
OP2	Transmitter Signal Element Timing (DTE Source)
OP3	Data Signal Rate Selector
OP4	Secondary Request To Send

The modem cable preserves the above configuration except that OP4 is not connected.

The two printer cables reconfigure the output port connections as follows:

Table 2-4. Output Port Printer Cable Connections

Output Port Pin	RS-232-C Signal Line
OP0	Clear To Send/Data Set Ready
OP1	Received Line Signal Detector
OP2	Transmitter Signal Element Timing (DCE Source)
OP3-OP4	Not Connected

The instrumentation cable reconfigures the output port connections as follows:

Table 2-5. Output Port Instrumentation Cable Connections

Output Port Pin	RS-232-C Signal Line
OP0	Clear To Send
OP1	Received Line Signal Detector
OP2	Transmitter Signal Element Timing (DCE Source)
OP3	Data Set Ready
OP4	Not Connected

Operating Modes. Each data channel can be independently programmed to operate in one of four operating modes. You can specify the channel A mode with bits 6 and 7 of Channel A Mode Register II. Use Channel B Mode Register II to specify the channel B mode.

The first mode is the *normal operating mode*, which allows each channel to operate in either simplex, half-duplex, or full duplex. In this mode the transmitter and receiver of each channel operate independently.

The second mode is the *auto-echo mode*. In this mode the received data can be read by the computer, but it is also automatically retransmitted. The following conditions are true in this mode:

1. All received data is reclocked and transmitted by the transmitter.
2. The baud rate selected for the receiver is automatically used for the transmitter.
3. The receiver must be enabled, but the transmitter need not be.
4. The "transmitter empty" and "transmitter ready" status bits are inactive.
5. Parity is checked if in use, but parity bits are just transmitted as received (not regenerated).
6. Character framing is checked, but the stop bits are just transmitted as received (not regenerated).
7. If a break is received, it is echoed just as received until the next valid start bit is received.
8. The computer cannot use a channel that is in auto-echo mode to transmit, only to receive.

The third mode of operation is a diagnostic mode known as *local loop-back mode*. When a channel is operating in this mode the following conditions are true:

1. The output of the transmitter is internally connected to the input of the receiver.
2. The baud rate selected for the transmitter is also used for the receiver.
3. The transmitter must be enabled, but the receiver need not be.
4. The Transmitted Data output is held in the marking state.
5. The Received Data input is ignored.
6. The computer can send data to the transmitter and should receive the same data back from the receiver.

The fourth mode of operation, the *remote loop-back mode*, is also a diagnostic mode. The following conditions are true when a channel is operating in this mode:

1. Data received from an external source is reclocked and transmitted back to the external source by the transmitter.
2. The baud rate selected for the receiver is also used for the transmitter.
3. The receiver must be enabled, but the transmitter need not be.
4. The computer does not have access to the received data and the status register error bits are inactive.
5. The received parity is not checked or regenerated. Parity bits are just transmitted as received.
6. Character framing is not checked. Stop bits are just transmitted as received.
7. A received break is echoed as received until the next valid start bit is detected.

Line Drivers and Receivers

Each UART output is interfaced to the corresponding pin in the interface's back-panel connector by a line driver. Each UART input is interfaced by a line receiver. These circuits provide compatibility with the voltage levels of RS-232-C signal lines as defined by the EIA RS-232-C standard.

2

RS-232-C Back-Panel Connector

The HP 82919A Serial Interface provides a male 25-pin D-subminiature connector wired in DTE configuration according to the RS-232-C standard. The pin configuration of this connector is as follows:

Table 2-6. Back-Panel Connector Pin Configuration

Pin No.	Signal Name	Signal Direction
1	Protective Ground	N/A
2	Transmitted Data	Interface to Device
3	Received Data	Device to Interface
4	Request To Send	Interface to Device
5	Clear To Send	Device to Interface
6	Data Set Ready	Device to Interface
7	Signal Ground	N/A
8	Received Line Signal Detector*	Device to Interface
9-11	No Connection	
12	Secondary Received Line Signal Detector	Device to Interface
13	Secondary Clear To Send	Device to Interface
14	Secondary Transmitted Data	Interface to Device
15	No Connection	

* Also called "Data Carrier Detect."

(Table continued on next page.)

Table 2-6. Back-Panel Connector Pin Configuration (continued)

Pin No.	Signal Name	Signal Direction
16	Secondary Received Data	Device to Interface
17-18	No Connection	
19	Secondary Request To Send	Interface to Device
20	Data Terminal Ready	Interface to Device
21	No Connection	
22	Ring Indicator	Device to Interface
23	Data Signal Rate Selector	Interface to Device
24	Transmitter Signal Element Timing (DTE Source)	Interface to Device
25	No Connection	

The four serial interface cables reconfigure the pin connections of the back-panel connector. The configuration of each cable is given in appendix A.

Registers

You can program the operation of the HP 82919A Serial Interface by accessing its hardware registers. *The procedures for reading or writing to a register depend on your operating system and programming language. Refer to your operating system and language documentation for the correct statements.* Whatever the access method, you will need to identify each register with its least-significant address byte. These address bytes are given in the register descriptions that follow.

If you accidentally specify the wrong least-significant address byte, you may access an illegal register address. You may lose some data if you do this, but no damage to the interface or computer will result. You can return your system to normal operation by performing a hardware reset.



The four available cables do not implement the secondary channel (channel B) signals. If you have an application that requires the second channel, you need to construct a special cable. Ignore the channel B registers unless you are using such a cable.

Register 0: Identification and Status

Register 0 contains the identification bits of the HP 82919A Serial Interface, and also indicates whether interrupts are enabled, the level at which the interface can interrupt the computer, and whether an interrupt is pending.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Interrupt Enable	Interrupt Pending	Interrupt Level		Identification Bits "0010"			

To access Register 0:

- Least-significant byte of address = 01 (hexadecimal).
- Read and write access is allowed for bits 4 through 7. Bits 0 through 3 are read only.

Bits 0 Through 3: Identification. These bits are permanently set to "0010" (2), the identification code for the HP 82919A Serial Interface.

Bits 4 and 5: Interrupt Level. These bits specify the level at which the interface can issue an interrupt to the computer. The following table gives the priority levels specified by various settings of these bits (in order of increasing priority):

Table 2-7. Interrupt Level

Bit 5	Bit 4	Interrupt Priority Level
0	0	0
0	1	1
1	0	2
1	1	3

Bit 6: Interrupt Pending. This bit, when equal to "1", indicates that an interrupt is pending. Bit 6 is a read/write bit. You can force a hardware interrupt by setting this bit to a "1" (provided interrupts are enabled).

Bit 7: Interrupt Enable. This bit, when set to a "1", enables the interrupting capability of the interface. Pending or forced interrupts are ignored when bit 7 is equal to "0".

Register 1: Channel A Mode Register I

This register and Channel A Mode Register II (Register 2) are both accessed by addressing hexadecimal 39. The channel A mode register pointer determines which register is accessed. You can set the pointer to mode register I by writing a "reset mode register pointer" command to the Channel A Command register (Write Register 7). A hardware reset also resets the pointer. The pointer advances to mode register II after mode register I has been accessed (read or write).

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Receiver Control of OP0	Receiver Interrupt Select	Error Mode Select	Parity Mode		Parity Type	Data Bits Per Character	

To access Register 1:

- Least-significant byte of address = 39 (hexadecimal).
- The channel A mode register pointer must be set at mode register I.
- The channel A transmitter and receiver must be reset before you change the contents of this register.
- Read and write access is allowed.

Bits 0 and 1: Data Bits Per Character. This field specifies the number of data bits per character for channel A:

Table 2-8. Data Bits Per Character

Bit 1	Bit 0	Number of Data Bits
0	0	5
0	1	6
1	0	7
1	1	8

Bit 2: Parity Type. Bit 2 specifies parity type for channel A. The effect of this bit depends upon the parity mode specified with bits 3 and 4. If "with parity" mode is selected, bit 2 equal to "0" specifies even parity, while "1" specifies odd parity. In "force parity" mode, bit 2 equal to "0" specifies "always zero" parity, while "1" specifies "always 1" parity.

Bits 3 and 4: Parity Mode. These bits specify channel A parity mode. If "with parity" or "force parity" is selected, a parity bit is added to each transmitted character and the receiver performs a parity check on the incoming data.

Table 2-9. Parity Mode

Bit 4	Bit 3	Parity Mode
0	0	With Parity
0	1	Force Parity
1	0	No Parity

Bit 5: Error Mode. This bit selects the operating mode for the "framing error," "parity error," and "received break" bits in the Channel A Status register (Read Register 5). If bit 5 is equal to "0", the *character* mode is selected and status is provided on a character-by-character basis. If bit 5 is a "1", *block* mode is selected. In block mode the three error bits indicate the logical OR of the status for all characters that have reached the top of the Channel A Receiver Buffer since the last "reset error status" command.

Bit 6: Receiver Interrupt Select. This bit selects the condition that results in a channel A receiver interrupt. If this bit is equal to "0", an interrupt is generated on the channel A "receiver ready" condition. If this bit is equal to "1", an interrupt is generated on a channel A "receiver buffer full" condition. (Refer to Read Register 12, the Interrupt Status register.)

Bit 7: Receiver Control of OP0. This bit, when set, enables the deactivation of the OP0 output by the channel A receiver. OP0 is asserted by setting bit 0 of the Output Port register (Register 10). If bit 7 of mode register I is equal to "1", OP0 is negated upon receipt of a valid start bit if the Channel A Receiver Buffer is full. However, bit 0 of Register 10 remains set.

- OP0 is connected to Data Terminal Ready in the back-panel RS-232 connector and the modem cable. Thus, once the receiver buffer is full, the Data Terminal Ready line is deactivated by the start bit of the next character (preventing an overrun error). Data Terminal Ready is reasserted once an empty receiver buffer position becomes available.
- OP0 is connected to Clear To Send in the instrumentation cable, and to both Clear To Send and Data Set Ready in the two printer cables.

Register 2: Channel A Mode Register II

This register, like Channel A Mode Register I, is accessed by addressing hexadecimal 39. The channel A mode register pointer moves to mode register II after mode register I has been accessed (read or write). Accessing mode register II does not change the pointer.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mode Select		Transmitter Control of OP0	IPO Control of Transmitter	Stop Bit Length			

To access Register 2:

- Least-significant byte of address = 39 (hexadecimal).
- The channel A mode register pointer must be set at mode register II.
- The channel A transmitter and receiver must be reset before you change the contents of this register.
- Read and write access is allowed.

Bits 0 Through 3: Stop Bit Length. These bits specify stop bit length.* You can specify a stop bit length of either 1.0 or 2.0 if you have specified six, seven, or eight data bits per character (refer to Register 1). If you have specified five data bits per character, use a stop bit length of 1.5. Table 2-10 gives the allowable selections:

Table 2-10. Stop Bit Length

Value Written to Bits 3-0	Data Bits Per Character	Stop Bit Length
0111	6, 7, or 8	1.0
0111	5	1.5
1111	6, 7, or 8	2.0

* You should always set bits 0, 1, and 2 equal to "1". Bit 3 can be equal to either "0" or "1".

Bit 4: IP0 Control of Transmitter. This bit enables the IP0 input to control the channel A transmitter. If bit 4 is equal to "0", IP0 has no effect on the transmitter. If bit 4 is equal to "1", the transmitter checks the state of IP0 each time it is ready to send a character. If IP0 is asserted (low), the character is transmitted. If IP0 is negated (high), the channel A transmitter output remains in the marking state and the transmission is delayed until IP0 goes low. Changes in IP0 while a character is being transmitted do not affect the transmission of that character.

- IP0 is connected to Clear To Send in the backpanel RS-232 connector and the modem cable. If bit 4 is equal to "1", the transmitter will output a character only if Clear To Send is asserted.
- IP0 is connected to Data Terminal Ready in the instrumentation and printer cables. If bit 4 is equal to "1", the transmitter will output a character only if Data Terminal Ready is asserted.

Bit 5: Transmitter Control of OP0. This bit, when set, enables deactivation of the OP0 output by the channel A transmitter. OP0 is asserted by setting bit 0 of the Output Port register (Register 10). If bit 5 of mode register II is equal to "1", bit 0 of Register 10 is reset to "0" automatically once all characters in the transmitter buffer and shift register have been transmitted (including stop bits). This feature can be used to automatically terminate the transmission of a message.

- OP0 is connected to Data Terminal Ready in the backpanel RS-232 connector and the modem cable. Thus, Data Terminal Ready is deactivated once all characters have been transmitted if bit 5 is equal to "1".

- OP0 is connected to Clear To Send in the instrumentation cable, and to both Clear To Send and Data Set Ready in the two printer cables.



For this feature to work, your program must disable the transmitter after the last character is transferred into the transmitter buffer.

Bits 6 and 7: Mode Select. These bits select the operating mode of UART channel A as shown in table 2-11. Refer to “Operating Modes” earlier in this chapter for a description of each of the four modes of UART operation. Note that channels A and B may be in different operating modes.

Table 2-11. Operating Modes

Bit 7	Bit 6	Operating Mode
0	0	Normal
0	1	Auto Echo
1	0	Local Loop Back
1	1	Remote Loop Back

Register 3: Channel B Mode Register I

This register and Register 4 (Channel B Mode Register II) are both accessed by addressing hexadecimal 29. The channel B mode register pointer determines which register is accessed. You can set the pointer to Channel B Mode Register I by writing a “reset mode register pointer” command to the Channel B Command register (Write Register 8). A hardware reset also resets the pointer. The pointer advances to mode register II after mode register I has been accessed (read or write).

To access Register 3:

- Least-significant byte of address = 29 (hexadecimal).
- The channel B mode register pointer must be set at mode register I.
- The channel B transmitter and receiver must be reset before you change the contents of this register.
- Read and write access is allowed.

The bit definitions for this register are identical to those of Channel A Mode Register I except for the following:

1. All control actions apply to the channel B transmitter and receiver.
2. Bit 7 controls deactivation of the OP1 output (rather than OP0) when the channel B receiver buffer is full. OP1 is connected to Request To Send in the backpanel RS-232 connector and the modem cable, and to Received Line Signal Detector in the instrumentation and printer cables.

Register 4: Channel B Mode Register II

This register, like Channel B Mode Register I, is accessed by addressing hexadecimal 29. The Channel B Mode Register pointer moves to mode register II after mode register I has been accessed (read or write). Accessing mode register II does not change the pointer.

To access Register 4:

- Least-significant byte of address = 29 (hexadecimal).
- The channel B mode register pointer must be set at mode register II.
- The channel B transmitter and receiver must be reset before you change the contents of this register.
- Read and write access is allowed.

The bit definitions for this register are identical to those for Channel A Mode Register II except for the following:

1. All control actions apply to the channel B transmitter and receiver.
2. Bit 4 enables the IP1 input to control the channel B transmitter rather than IP0 to control the channel A transmitter. IP1 is connected to Data Set Ready in the back-panel RS-232 connector and the modem cable. IP1 is not connected if you are using the instrumentation cable. IP1 is connected to Data Terminal Ready in the printer cables.
3. Bit 5, when set, enables the deactivation of OP1 (rather than OP0) by the transmitter. OP1 is connected to Request To Send in the back-panel connector and modem cable, and to Received Line Signal Detector in the instrumentation and printer cables.

Read Register 5: Channel A Status

This register provides the current status of the channel A transmitter and receiver. The contents of this register are cleared to zero by a hardware reset.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Received Break	Framing Error	Parity Error	Overrun Error	Transmitter Empty	Transmitter Ready	Receiver Buffer Full	Receiver Ready

To access Read Register 5:

- Least-significant byte of address = 3B (hexadecimal).
- Read-only access is allowed.

Bit 0: Receiver Ready. This bit, when equal to "1", indicates that a character has been received and is waiting in the Channel A Receiver Buffer to be read by the computer. Bit 0 is cleared to "0" after the last character is read from the buffer.

Bit 1: Receiver Buffer Full. This bit, when equal to "1", indicates that all three character positions in the Channel A Receiver Buffer are occupied. Reading the receiver buffer clears this bit to "0" (unless another character is waiting in the receiver shift register).

Bit 2: Transmitter Ready. This bit, when equal to "1", indicates that the Channel A Transmitter Buffer is empty. This bit is cleared when a character is written to the transmitter buffer, and is set when the character is transferred to the transmitter shift register.

Bit 3: Transmitter Empty. This bit is set equal to "1" when the channel A transmitter underruns. That is, when both the transmitter buffer and transmitter shift register are empty.

Bit 4: Overrun Error. This bit, when set, indicates that the channel A receiver has overrun. This occurs when the receiver buffer is filled with three characters, a fourth character is in the receiver shift register, and the start bit of a fifth character is received. The character in the shift register (the fourth character) is lost.

Bit 5: Parity Error. When channel A is in "with parity" or "force parity" mode, bit 5 is set upon receipt of a character with incorrect parity.

Bit 6: Framing Error. This bit, when set, indicates that a stop bit was not detected in an incoming character.

Bit 7: Received Break. This bit, when set, indicates a break condition has been detected by channel A. A break is indicated when an all zero character of the programmed length is received without a stop bit. When this bit is set, the channel A "change in break" bit in the Interrupt Status register (Read Register 12) is also set.



If the Channel A Status register is read when there are no characters in the receiver buffer (bit 0 = 0), bits 5 through 7 ("parity error," "framing error," and "received break") remain in whatever state they were in for the last character received. These bits are updated when a new character is placed in the receiver buffer.

Write Register 5: Channel A Baud Rate Select

This register selects the baud rate for the channel A transmitter and receiver.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Receiver Baud Rate Select				Transmitter Baud Rate Select			

To access Write Register 5:

- Least-significant byte of address = 3B (hexadecimal).
- Write-only access is allowed.

Bits 0 Through 3: Transmitter Baud Rate Select. You may select one of 18 standard baud rates for the channel A transmitter by writing to this field, or you may specify the timer as the baud rate source. To specify a baud rate, write the appropriate value to bits 0 through 3 of this register and to bit 7 of the Auxiliary Control register (Write Register 11), as shown in table 2-12:

Table 2-12. Baud Rate Selection

Baud Rate Select Register Bits 3–0	Baud Rate	
	Auxiliary Control Register Bit 7 = 0	Auxiliary Control Register Bit 7 = 1
0000	50	75
0001	110	110
0010	134.5	134.5
0011	200	150
0100	300	300
0101	600	600
0110	1200	1200
0111	1050	2000
1000	2400	2400
1001	4800	4800
1010	7200	1800
1011	9600	9600
1100	38,400	19,200
1101	Timer	Timer

If you select the timer (binary 1101), the baud rate is determined by the 16-bit divisor contained in Registers 13 and 14. This allows you to select a non-standard baud rate.



Although you can select a baud rate of 38,400, operation at this rate is not supported.

Bits 4 Through 7: Receiver Baud Rate Select. This field selects the channel A receiver baud rate (in conjunction with bit 7 of the Auxiliary Control register). The baud rate selections are exactly as listed for the transmitter in table 2-12, except that the control bits are written to the upper four bits rather than the lower four bits of the register.

Read Register 6: Channel B Status

This register provides the current status of the channel B transmitter and receiver. The contents of this register are cleared to zero by a hardware reset.

To access Read Register 6:

- Least-significant byte of address = 2B (hexadecimal).
- Read-only access is allowed.

The bit definitions of this register are identical to those of the Channel A Status register (Read Register 5) except that they apply to channel B.

Write Register 6: Channel B Baud Rate Select

This register selects the baud rate for the channel B transmitter and receiver.

To access Write Register 6:

- Least-significant byte of address = 2B (hexadecimal).
- Write-only access is allowed.

The baud rate selection procedure for channel B is the same as for channel A (Write Register 5).

Write Register 7: Channel A Command

You can use this register to send commands to UART channel A. You can specify multiple commands in a single write to the register as long as the commands are not in conflict with each other.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Not Used	Miscellaneous Commands			Disable Transmitter	Enable Transmitter	Disable Receiver	Enable Receiver

To access Write Register 7:

- Least-significant byte of address = 3D (hexadecimal).
- Write-only access is allowed.

Bit 0: Enable Receiver. Setting this bit enables operation of the channel A receiver and causes the receiver to initiate a search for a start bit.

Bit 1: Disable Receiver. Setting this bit terminates operation of the receiver immediately—a character being received will be lost. The command has no effect on the receiver status bits or any other control registers.

Bit 2: Enable Transmitter. Setting this bit enables the channel A transmitter and asserts the “transmitter ready” status bit.

Bit 3: Disable Transmitter. Setting this bit terminates channel A transmitter operation and resets the “transmitter ready” and “transmitter empty” status bits. However, the transmitter will finish sending any characters currently in the transmitter buffer and shift register before becoming inactive.

Bits 4 Through 6: Miscellaneous Commands. The value of this three-bit field specifies a single command. The values and commands are listed in the following table:

Table 2-13. Miscellaneous Commands

Bits 6-4	Command
000	<i>No command.</i>
001	<i>Reset mode register pointer.</i> Resets the channel A mode register pointer to mode register 1.
010	<i>Reset receiver.</i> Disables the channel A receiver and clears the receiver buffer (as if a hardware reset has occurred).
011	<i>Reset transmitter.</i> Resets the channel A transmitter as if a hardware reset has occurred.
100	<i>Reset error status.</i> Clears the "received break," "parity error," "framing error," and "overrun error" bits in the Channel A Status register.
101	<i>Reset break change interrupt.</i> Clears the "channel A change in break" bit in the Interrupt Status register (Read Register 12).
110	<i>Start break.</i> Forces the channel A transmitter data output to the spacing state. If the transmitter is active, the break will be delayed until any characters in the transmitter buffer or shift register have been sent. The transmitter must be enabled for this command to be accepted.
111	<i>Stop break.</i> Forces the channel A transmitter data output to the marking state. This output will remain in the marking state for one bit time before the next character, if any, is sent.

Bit 7: Unused. This bit *must* always remain equal to zero. Setting this bit may cause unpredictable UART operation.

Write Register 8: Channel B Command

You can use this register to send commands to UART channel B.

To access Write Register 7:

- Least-significant byte of address = 2D (hexadecimal).
- Write-only access is allowed.

The bit definitions of this register are the same as those of the Channel A Command register except that all commands apply to channel B.

Read Register 9: Input Port

This register indicates the state of the RS-232-C signal lines connected to input port pins IP0 through IP5.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Always 1	Always 1	IP5	IP4	IP3	IP2	IP1	IP0

To access Read Register 9:

- Least-significant byte of address = 23 (hexadecimal).
- Read-only access is allowed.

The input port pins IP0 through IP5 and the RS-232-C signal lines connected to them are covered under the subheading "Input Port" in this chapter.

Bits 0 through 5 of this register indicate the state (active or inactive) of the RS-232-C signal lines connected to pins IP0 through IP5, respectively. *Negative true logic is used.* A bit equal to "1" indicates that the corresponding signal line is inactive. A bit equal to "0" indicates that the corresponding signal line is active.

For example, if you are using the modem cable, pin IP0 is connected to the Clear To Send signal line. If the Clear To Send line is active, bit 0 of the input port register will be equal to "0".

**Write Register 9:
Output Port
Configuration**

This register controls the function of UART output port pins OP2 through OP7. However, the only reconfiguration that is allowed by the interface circuit is the selection of either the $\times 1$ or $\times 16$ channel A clock signal for output OP2.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Always "0"						OP2 Clock Select	

To access Write Register 9:

Least-significant byte of address = 23 (hexadecimal).

Write-only access is allowed.

Bits 0 and 1: OP2 Clock Select. This field selects the clock signal to be output by OP2. OP2 is connected to the Transmitter Signal Element Timing (DTE source) RS-232-C signal line in the back-panel connector and modem cable, and to the Transmitter Signal Element Timing (DCE source) line in the printer and instrumentation cables. You may choose either of two clock signals:

Table 2-14. OP2 Configuration

Bit 1	Bit 0	OP2 Clock Output
0	1	<i>Channel A transmitter $\times 16$ clock.</i> If data is not being output, a free-running $\times 16$ clock signal is output. This is the normal function of the OP2 output.
1	0	<i>Channel A transmitter $\times 1$ clock.</i> If data is not being output, a free-running $\times 1$ clock signal is output. The $\times 1$ clock is the proper clock signal for Bell 212A modems and other modems that require an external clock signal.

Bits 2 Through 7. These bits must always be equal to "0" so that the OP0, OP1, OP3, and OP4 outputs will be programmed to be under Output Port register (Register 10) control.

Register 10: Output Port

You can use this register to specify the state of the RS-232-C signal lines connected to OP0, OP1, OP3, and OP4. (The OP2 output is configured as a clock signal and OP5 through OP7 are not used.)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OP7 (Not Used)	OP6 (Not Used)	OP5 (Not Used)	OP4	OP3	OP2 (Clock)	OP1	OP0

To access Register 10:

- This register cannot be directly accessed.
- Use the “set output port bits” command to set bits in Register 10 equal to “1”.
- Use the “reset output port bits” command to clear bits in Register 10 to “0”.

Refer to “Output Port” in this chapter for a description of outputs OP0 through OP4 and the RS-232-C signal lines connected to them.

Bits 0, 1, 3, and 4. These bits specify the state (active or inactive) of the RS-232-C signal lines connected to the OP0, OP1, OP3, and OP4 UART outputs, respectively. *Positive true logic is used.* That is, if you set a bit in the Output Port register equal to “1”, the corresponding signal line becomes active. If you reset a bit to “0”, the corresponding signal line becomes inactive. Refer to the “Output Port” subsection for the signal line configurations with each interface cable.

Bits 2, 5, 6, and 7. These bits should always be equal to "0".

You must use the "set output port bits" and "reset output port bits" commands to set and reset bits in the Output Port register. You cannot write values directly to the register.

The "Set Output Port Bits" Command. This command allows you to set bits in the Output Port register equal to "1" (activating the corresponding signal lines). You can execute the "set output port bits" command by writing the desired control byte to hexadecimal address byte 25. Bits 7 through 0 in the control byte affect bits 7 through 0 in the Output Port register, respectively:

- A bit equal to "1" in the control byte sets the corresponding bit in the Output Port register.
- A bit equal to "0" in the control byte leaves the corresponding bit in the register in its original state ("0" or "1").

For example, the control byte "00000011" leaves Output Port register bits 7 through 2 in their original states and sets bits 1 and 0 equal to "1".

The "Reset Output Port Bits" Command. This command allows you to reset bits in the Output Port register to "0" (deactivating the corresponding signal lines). You can execute the "reset output port bits" command by writing the desired control byte to hexadecimal address byte 27. Bits 7 through 0 in the control byte affect bits 7 through 0 in the Output Port register, respectively:

- A bit equal to "1" clears the corresponding bit in the register.
- A bit equal to "0" leaves the corresponding bit in the register in its original state.

A hardware reset of the interface resets all bits of the Output Port register to "0".

An example is in order. The Data Terminal Ready signal line is connected to output port pin OP0 in the back-panel connector and modem cable. The state of this line is controlled by bit 0 of the Output Port register. If bit 0 is equal to "0" (as it would be after a hardware reset), the Data Terminal Ready line is inactive. You can activate Data Terminal Ready by setting this bit to a "1" with the "set output port bits" command.

Read Register 11: Input Port Change

This register provides information on the changes of state that may occur for pins IP0 through IP3.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Delta IP3	Delta IP2	Delta IP1	Delta IP0	IP3	IP2	IP1	IP0

To access Read Register 11:

- Least-significant byte of address = 31 (hexadecimal).
- Read-only access is allowed.

Bits 0 Through 3: IP0–IP3 Current State. These bits provide the current state of the RS-232-C signal lines connected to UART inputs IP0 through IP3. *Negative true logic is used.* A "1" indicates an inactive signal line (as with the Input Port register).

Bits 4 Through 7: IP0–IP3 Change Of State. Each of these bits is set to a “1” when a change of state occurs at the corresponding input signal line. A change of state can be either a low-to-high or high-to-low transition lasting at least 50 microseconds. You can enable an interrupt for a change of state of one or more of these inputs. Bits 4 through 7 are cleared by a hardware reset or when the register is read.

Write Register 11: Auxiliary Control

This register provides a set of auxiliary commands that you may use to control the UART.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Baud Rate Select	Timer Clock Source			Delta IP3 Interrupt	Delta IP2 Interrupt	Delta IP1 Interrupt	Delta IP0 Interrupt

To access Write Register 11:

- Least-significant byte of address = 31 (hexadecimal).
- Write-only access is allowed.

Bits 0 Through 3: Change of State Interrupt

Enable. These bits correspond to the IP0 through IP3 inputs. If an enable bit is set, bit 7 of the Interrupt Status register (Read Register 12) will be set when the corresponding input undergoes a change of state. An interrupt will result if bit 7 of the Interrupt Mask register (Write Register 12) is set.

Bits 4 Through 6: Timer Clock Source. This field selects the clock source that drives the timer. You may select either the crystal oscillator or the crystal oscillator divided by 16 as the clock source:

Table 2-15. Timer Clock Source

Bits 6–4	Clock Source
110	Oscillator divided by 1.
111	Oscillator divided by 16.

Bit 7: Baud Rate Select. This bit is used in conjunction with the Channel A and B Baud Rate Select registers (Write Registers 5 and 6) to select baud rates. Refer to these registers for the available baud rates.

**Read Register 12:
Interrupt Status**

This register provides the status of eight potential interrupt sources. The contents of this register are masked by the Interrupt Mask register (Write Register 12). If a bit in the Interrupt Status register is set, an interrupt will occur only if the corresponding bit in the Interrupt Mask register is also set.

A hardware reset clears all bits in this register.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Input Port Change	Channel B Change In Break	Channel B Receiver Ready/ Receiver Buffer Full	Channel B Trans-mitter Ready	Not Used (Ignore)	Channel A Change In Break	Channel A Receiver Ready/ Receiver Buffer Full	Channel A Trans-mitter Ready

To access Read Register 12:

- Least-significant byte of address = 33 (hexadecimal).
- Read-only access is allowed.

Bit 0: Channel A Transmitter Ready. This bit is a duplicate of bit 2 of the Channel A Status register (Read Register 5).

Bit 1: Channel A Receiver Ready or Receiver Buffer Full. The function of this bit is programmed by bit 6 of Channel A Mode Register I (Register 1). Bit 1 can be either a duplicate of bit 0 ("receiver ready") or bit 1 ("receiver buffer full") of the Channel A Status register (Read Register 5).

Bit 2: Channel A Change In Break. This bit is set when the channel A receiver detects the beginning or end of a received break. It is reset by the "reset break change interrupt" command (refer to Write Register 7, the Channel A Command register).

Bit 3: Not Used. Ignore the value of this bit (usually "1").

Bit 4: Channel B Transmitter Ready. This bit is a duplicate of bit 2 of the Channel B Status register (Read Register 6).

Bit 5: Channel B Receiver Ready or Receiver Buffer Full. The function of this bit is programmed by bit 6 of Channel B Mode Register I (Register 3). Bit 1 can be either a duplicate of bit 0 ("receiver ready") or bit 1 ("receiver buffer full") of the Channel B Status register (Read Register 6).

Bit 6: Channel B Change In Break. This bit operates just as bit 2 does for channel A.

Bit 7: Input Port Change. This bit is set equal to “1” when a change of state has occurred at the IP0, IP1, IP2, and/or IP3 inputs *if the corresponding bit in the Auxiliary Control register (Write Register 11) has been set*. This bit is cleared when the Input Port Change register (Read Register 11) is read.

Write Register 12: Interrupt Mask

You can enable interrupts for the bits in the Interrupt Status register by setting the corresponding bits in the Interrupt Mask register. If the bit in the Interrupt Mask register is equal to “1”, an interrupt will occur when the corresponding bit in the Interrupt Status register is set.

A hardware reset clears all bits in this register.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Input Port Change Interrupt	Channel B Change In Break Interrupt	Channel B Receiver Ready/ Receiver Buffer Full Interrupt	Channel B Transmitter Ready Interrupt	Not Used (Always “0”)	Channel A Change In Break Interrupt	Channel A Receiver Ready/ Receiver Buffer Full Interrupt	Channel A Transmitter Ready Interrupt

To access Write Register 12:

- Least-significant byte of address = 33 (hexadecimal).
- Write-only access is allowed.



Bit 3 of this register *must* always be equal to “0”. If you set this bit, an interrupt may occur on every clock cycle!

Registers 13 and 14: Timer Divisor Latch

These registers together make up the 16-bit divisor latch for the timer. Register 13 contains the *most-significant byte*; Register 14, the *least-significant byte*.

2

To access Registers 13 and 14:

- Register 13: Least-significant address byte = 35 (hexadecimal).
- Register 14: Least-significant address byte = 37 (hexadecimal).
- Read and write access is allowed for both registers. However, reading these registers will produce the current count, not the original value. Reading these registers is not recommended.

You can use the timer to provide any desired baud rate in the operating range of the interface. The baud rate is determined by the 16-bit divisor contained in Registers 13 and 14, which divides the frequency of the timer's clock source. Since you may specify either the crystal oscillator divided by 1 or divided by 16 as the clock source for the timer, there are two equations for determining the divisor. If you are using the oscillator divided by 1, the equation is:

$$\text{Divisor} = 115,200 \div \text{Baud Rate}$$

If you are using the oscillator divided by 16, the following equation should be used:

$$\text{Divisor} = 7,200 \div \text{Baud Rate}$$

In either case, you should separate the 16 bits of the divisor into two bytes. Write the most-significant byte to Register 13 and the least-significant byte to Register 14. Calculate the values to write to these registers as follows:

$$\text{Register 13 value} = \text{Integer part of } (\text{Divisor} \div 256)$$

$$\text{Register 14 value} = (\text{Divisor}) \bmod 256$$

If new values are written to Registers 13 and 14, the baud rate will change to the new rate once the current half cycle of the timer is completed.

A hardware reset will cause the timer to stop. You must execute a "start timer" command after a hardware reset. To do this, simply read address byte 25 (hexadecimal). A value of FF (hexadecimal) is returned and the timer starts.

Read Register 15: Channel A Receiver Buffer

The receiver buffer is the three-character first-in-first-out (FIFO) stack described under the subheading "Receiver Operation." Incoming data enters the FIFO stack from the receiver shift register. When you read this register, the character at the top of the stack (the first received) is returned. If the stack is empty, the value FF (hexadecimal) is returned.

To access Read Register 15:

- Least-significant byte of address = 3F (hexadecimal).
- Read-only access is allowed.

Write Register 15: Channel A Transmitter Buffer

The transmitter buffer is described under the subheading "Transmitter Operation." Data written to this register is transferred to the transmitter shift register, serialized, and transmitted.

To access Write Register 15:

- Least-significant byte of address = 3F (hexadecimal).
- Write-only access is allowed.

Read Register 16: Channel B Receiver Buffer

This register is analogous to the Channel A Receiver Buffer.

To access Read Register 16:

- Least-significant byte of address = 2F (hexadecimal).
- Read-only access is allowed.

Write Register 16: Channel B Transmitter Buffer

This register is analogous to the Channel A Transmitter Buffer.

To access Write Register 16:

- Least-significant byte of address = 2F (hexadecimal).
- Write-only access is allowed.

A

The Serial Interface Cables

Four cables are available to connect peripheral devices to the HP 82919A Serial Interface:

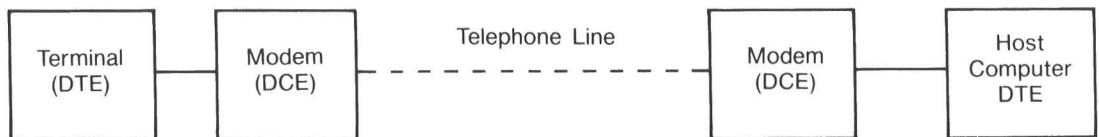
- HP 82974A Modem Cable F/M.
- HP 82974B Instrumentation Cable F/F.
- HP 82974C Serial Printer Cable F/F.
- HP 82974D Serial Printer Cable F/M.

The cable that you need depends upon your peripheral device.

Choosing a Cable

Before you can choose a cable to connect your peripheral, you must determine whether the peripheral is configured as Data Terminal Equipment (DTE) or Data Communications Equipment (DCE). All serial peripherals are classified as either DTE or DCE. The following figure shows how DTE and DCE devices are connected together to form a data communications network:

Figure A-1.
Data Communications
Network



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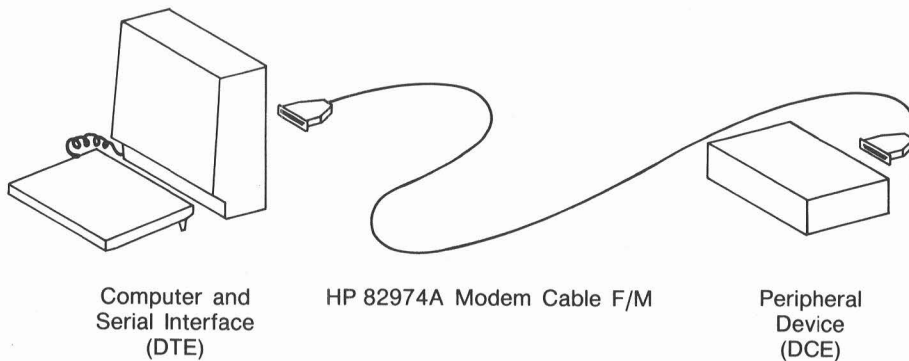
Connecting Data Communications Equipment

Data Terminal Equipment includes any device through which information can enter or exit a data communications network. Most terminals and printers are configured as DTE. Remote instrumentation is also often configured as DTE.

Data Communications Equipment is used to convey information between locations. Modems are configured as DCE.

If you are connecting a DCE peripheral (for example, a modem), use the HP 82974A Modem Cable F/M. The back-panel connector of the HP 82919A Serial Interface configures the interface and computer as DTE. The modem cable maintains this DTE configuration, allowing you to connect any DCE peripheral:

**Figure A-2.
Connecting a DCE
Peripheral**



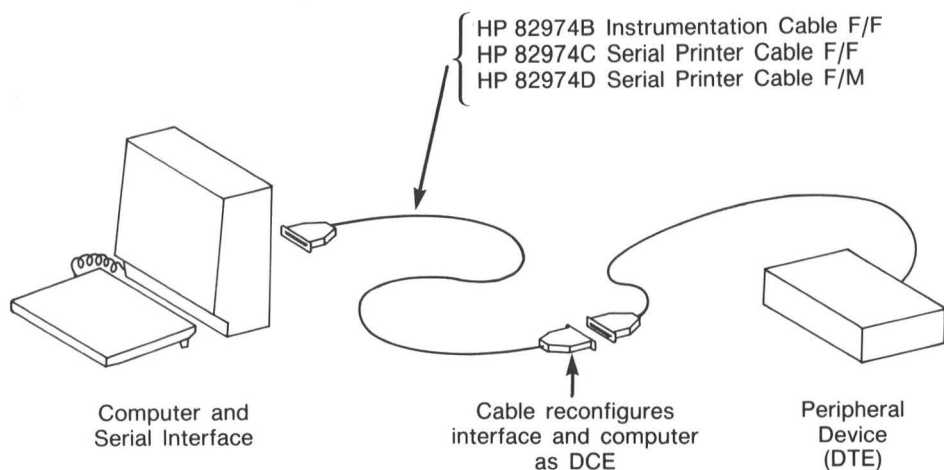
Connecting Data Terminal Equipment

If you are connecting a DTE peripheral (for example, a printer or terminal), use one of the following cables:

- HP 82974B Instrumentation Cable F/F.
- HP 82974C Serial Printer Cable F/F.
- HP 82974D Serial Printer Cable F/M.

These three cables reconfigure the serial interface as a DCE device. That is, the configuration at the *peripheral end* of the cable is DCE. This allows you to connect printers, terminals, and other DTE devices:

Figure A-3.
Connecting a DTE
Peripheral



The following table gives typical applications for the instrumentation and printer cables:

Table A-1. Cable Applications

Cable	Typical Applications
HP 82974B Instrumentation Cable F/F	Specialized applications involving DTE instrumentation.*
HP 82974C Serial Printer Cable F/F	Most non-HP serial printers and terminals. Most other DTE peripherals.
HP 82974D Serial Printer Cable F/M	Hewlett-Packard serial printers and terminals.
* The instrumentation cable is used where separate control of each RS-232-C line is needed. Refer to "Cable Configurations."	

If you are uncertain about which cable to use for your peripheral device, you may need to determine the device's pin configuration (refer to the owner's manual). Compare this pin configuration with that of the serial interface cables (refer to "Cable Configurations"). You may also want to contact your Hewlett-Packard dealer.

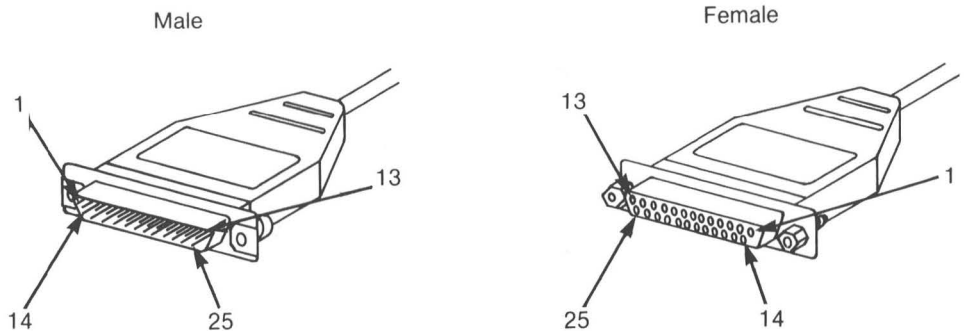
Cable Configurations

The four serial interface cables differ in two ways:

1. The connector at the peripheral end of the cable may be either male or female.
2. The cables have different pin configurations.

Although the RS-232-C standard does not specify a connector, the industry has adopted the male and female 25-pin D-subminiature connectors as “RS-232” standard connectors. Most DTE devices use the male connector, while DCE devices use the female connector. Figure A-4 illustrates the standard 25-pin connectors and identifies the pins:

Figure A-4.
RS-232 Connectors



The serial interface is wired as a DTE device according to the RS-232-C standard and provides a male 25-pin D-subminiature connector on its back panel. The pin configuration of the back-panel connector is given in chapter 2.

A

Each of the four serial interface cables has a female 25-pin connector at one end (to plug into the serial interface) and either a male or female 25-pin connector at the other end (to plug into the peripheral device). The name of each cable indicates the type of connector at each end. For example, the HP 82974A Modem Cable F/M has a female connector at the interface end and a male connector at the peripheral end, as indicated by "F/M."

The configurations of the individual cables are covered next.

**The HP 82974A
Modem Cable F/M**

The HP 82974A Modem Cable F/M preserves the DTE configuration of the serial interface and provides a 25-pin male connector at the peripheral end. The pin configuration of this cable is given in the following table:

Table A-2. Modem Cable Pin Configuration

Pin No.	Signal Name	Signal Direction
1	Protective Ground	N/A
2	Transmitted Data	Interface to Device
3	Received Data	Device to Interface
4	Request To Send	Interface to Device
5	Clear To Send	Device to Interface
6	Data Set Ready	Device to Interface
7	Signal Ground	N/A
8	Received Line Signal Detector*	Device to Interface
9-19	No Connection	
20	Data Terminal Ready	Interface to Device
21	No Connection	
22	Ring Indicator	Device to Interface
23	Data Signal Rate Selector	Interface to Device
24	Transmitter Signal Element Timing (DTE Source)	Interface to Device
25	No Connection	
* Also called "Data Carrier Detect."		

This pin configuration is the same as that of the back-panel connector (refer to chapter 2) except that the secondary channel signal lines are not connected. If you want to use the secondary data channel, you will have to construct a special cable.

The DTE configuration provided by the modem cable allows you to connect any single channel DCE device to the serial interface. See figure 1-1 for a typical application.

The HP 82974B Instrumentation Cable F/F

The HP 82974B Instrumentation Cable F/F reconfigures the interface as DCE and provides separate control of each line. The cable has female 25-pin connectors at both ends. Table A-3 gives the pin configuration of the connector at the *peripheral end*:

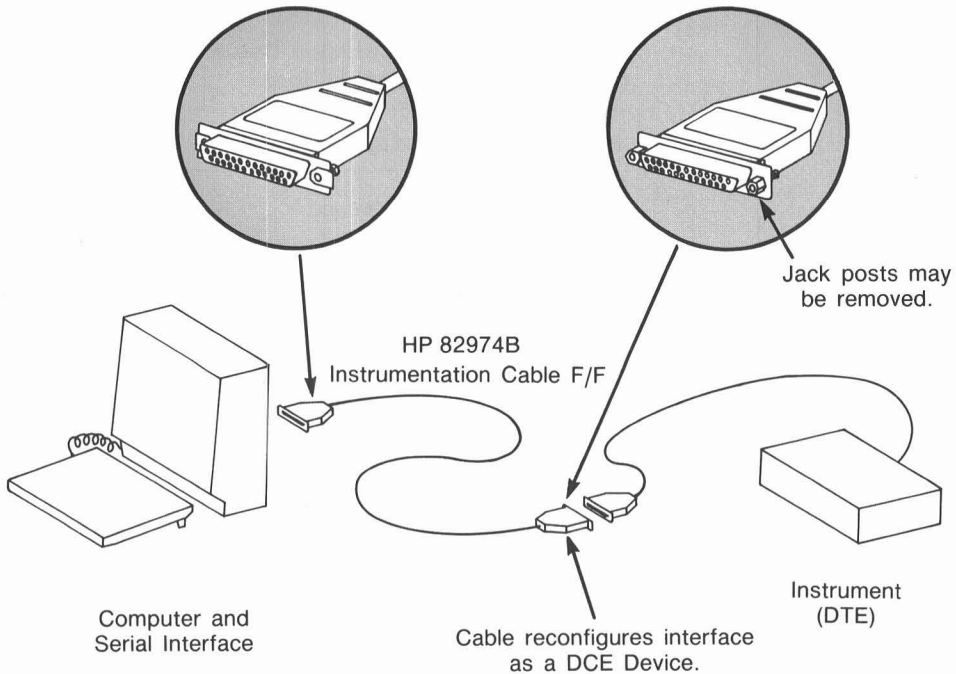
**Table A-3. Instrumentation Cable Pin Configuration
(Connector at Peripheral End)**

Pin No.	Signal Name	Signal Direction
1	Protective Ground	N/A
2	Transmitted Data	Device to Interface
3	Received Data	Interface to Device
4	Request To Send	Device to Interface
5	Clear To Send	Interface to Device
6	Data Set Ready	Interface to Device
7	Signal Ground	N/A
8	Received Line Signal Detector	Interface to Device
9-14	No Connection	
15	Transmitter Signal Element Timing (DCE Source)	Interface to Device
16-19	No Connection	
20	Data Terminal Ready	Device to Interface
21-25	No Connection	

The instrumentation cable is intended for certain specialized applications where separate control of each signal line is required. You can use the instrument cable if you are writing your own application programs in HP-UX Technical BASIC, or if you are writing your own low-level driver program. For other applications involving DTE peripheral devices, you should use one of the printer cables.

Figure A-5 shows how to connect a DTE device with the instrumentation cable:

**Figure A-5.
Instrumentation Cable
Connections**





The HP 82974B Instrumentation Cable F/F has female connectors at both ends. The connector at the interface end of the cable has retainer screws (to fasten the connector to the interface's back-panel connector), while the connector at the peripheral end has jack posts (to connect with an in-line male connector). *These connectors are not equivalent.* The pin configuration is different at each end of the cable. You can remove the jack posts from the connector at the peripheral end of the cable, but you need to mark the connectors so that you can tell them apart.

The HP 82974C Serial Printer Cable F/F

The HP 82974C Serial Printer Cable F/F, like the instrumentation cable, reconfigures the serial interface as DCE and has female 25-pin connectors at both ends. This cable provides a different pin configuration than the instrumentation cable:

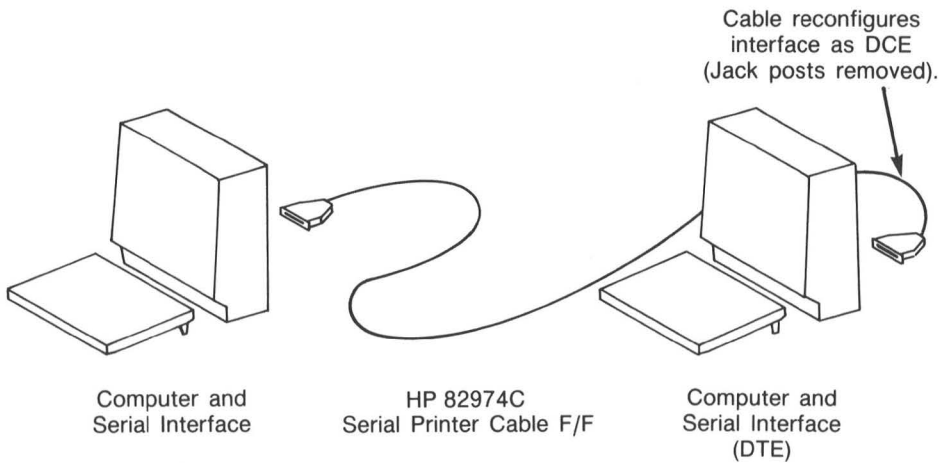
**Table A-4. Printer Cable Pin Configuration
(Connector at Peripheral End)**

Pin No.	Signal Name	Signal Direction
1	Protective Ground	N/A
2	Transmitted Data	Device to Interface
3	Received Data	Interface to Device
4	Request To Send	Device to Interface
5,6	Clear To Send, Data Set Ready	Interface to Device
7	Signal Ground	N/A
8	Received Line Signal Detector	Interface to Device
9-14	No Connection	
15	Transmitter Signal Element Timing (DCE Source)	Interface to Device
16-19	No Connection	
20	Data Terminal Ready	Device to Interface
21-25	No Connection	

Note that pins 5 and 6 are connected together in the HP 82974C Serial Printer Cable F/F. Your computer's operating system may require this. If your application requires separate control of each line, use the HP 82974B Instrumentation Cable F/F.

Figure 1-3 in chapter 1 shows how to connect a printer (or terminal) to the serial interface with the HP 82974C Serial Printer Cable F/F. This cable can be used for many other applications involving DTE peripherals. One application is to connect two computers together using two serial interfaces:

Figure A-6.
Connecting Two Comput-
ers Together



The HP 82974C Serial Printer Cable F/F, like the instrumentation cable, has female connectors at both ends. *These connectors are not equivalent.* The pin configuration is different at each end of the cable. You can remove the jack posts from the connector at the peripheral end of the cable, but you need to mark the connectors so that you can tell them apart.

The HP 82974D Serial Printer Cable F/M

The HP 82974D Serial Printer Cable F/M has the same pin configuration as the HP 82974C Serial Printer Cable F/F (refer to table A-4), but has a *male* 25-pin connector at the peripheral end. This is to connect with the female 25-pin connector mounted on Hewlett-Packard serial printers and terminals. Figure 1-2 in chapter 1 shows a typical application of this cable.

Special Cables

You may have an application that requires a special cable. For example, you may need to use the secondary channel (channel B) signal lines. These signals are available at the interface back-panel connector, but are not implemented by the four available cables. If you want to implement the secondary channel signal lines, you will need to construct your own cable. You can also construct a special cable if your peripheral has a non-standard pin configuration.

If you need to construct a special cable, refer to chapter 2 for the pin configuration of the back-panel connector of the serial interface. You may also need to refer to the manual supplied with your peripheral for the pin configuration of its connector.

B

CCITT Equivalents for RS-232-C Circuit Designations

This manual uses the RS-232-C designations for the serial interface data and signal lines. For each RS-232-C designation, there is an equivalent CCITT (Consultative Committee for International Telephone and Telegraph) designation. The following table gives the CCITT equivalent for each RS-232-C designation, and gives the pin number of each circuit in the serial interface back-panel connector.

Table B-1. CCITT and RS-232-C Equivalent Designations

CCITT Designation	RS-232-C Designation	Pin No.
101: Protective Ground	AA: Protective Ground	1
102: Common Return	AB: Signal Ground	7
103: Transmitted Data	BA: Transmitted Data	2
104: Received Data	BB: Received Data	3
105: Request To Send	CA: Request To Send	4
106: Ready For Sending	CB: Clear To Send	5
107: Data Set Ready	CC: Data Set Ready	6
108.2: Data Terminal Ready	CD: Data Terminal Ready	20
109: Data Channel Received Line Signal Detector	CF: Received Line Signal Detector	8
111: Data Signalling Rate Selector	CH: Data Signal Rate Selector	23
113: Transmitter Signal Element Timing (DTE)	DA: Transmit Signal Element Timing (DTE)	24
118: Transmitted Backward Channel Data	SBA: Secondary Transmitted Data	14
119: Received Backward Channel Data	SBB: Secondary Received Data	16
120: Transmit Backward Channel Line Signal	SCA: Secondary Request To Send	19
121: Backward Channel Ready	SCB: Secondary Clear To Send	13
122: Backward Channel Received Line Signal Detector	SCF: Secondary Received Line Signal Detector	12
125: Calling Indicator	CE: Ring Indicator	22

1

Setting Up the Interface (page 1-1)

2

Hardware Description (page 2-1)

A

Appendices (page A-1)

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